

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:)
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Kawasaki, et al.)
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Serial No.: 10/) Examiner: El Hady, N.
)
Filed: April 13, 2004) Group Art Unit: 2154
)
For: SINGLE-CHIP MICROCOMPUTER)
)

Mail Stop Patent Application
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. 1.97 and 1.98, and in compliance with 37 C.F.R. 1.56, the Office's attention is directed to the patents, publications and other information listed on the attached PTO-1449. Copies of such were previously provided or cited by the Patent Office in the parent application(s) upon which this application relies for an earlier filing date under 35 U.S.C. 120:

USSN: 09/055,099	Filed: 04/03/98	USP: 5,930,523	Issued: 07/27/99
USSN: 09/192,093	Filed: 11/13/98	USP: 6,223,265	Issued: 04/24/01
USSN: 09/191,313	Filed: 11/13/98	USP: 6,212,620	Issued: 04/3/01
USSN: 09/467,087	Filed: 12/10/99	USP: 6,279,063	Issued: 08/21/01
USSN: 09/918,625	Filed: 07/30/01	USP: 6,591,294	Issued: 07/08/03

or are already present in co-pending divisional/continuing applications of above parent:

USSN: 10/172,290 Filed: 06/13/02

Therefore, copies of the listed references are not provided herewith.

Regarding the documents, publications or other information listed on the attached PTO-1449, Applicant(s) believe(s) the same may qualify as "prior" art to this application and should be treated accordingly, although Applicant(s) reserve(s) the right to contest the prior art status of any document, publication or information cited herein.

Pursuant to 37 C.F.R. 1.97(b), this Statement is being filed within three months of the filing date of this application or before the mailing date of a first Office Action on the merits. If this Statement is not filed before the mailing date of a first office Action on the merits, the required certification is given below or, in the absence thereof, the Office is authorized to charge the required fee set forth in 37 C.F.R. 1.17(p) to Deposit Account No. 50-0251 for consideration of this Statement.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-0251.

Respectfully submitted,




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CERTIFICATE OF MAILING

I hereby certify that the foregoing is being deposited with the U.S. Postal Service by Express Mail, Label No. EV14235550US to Mail Stop Patent Application, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 this 13th day of April, 2004.


Karen A. Rogers

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(REV. 7-92)U.S. DEPARTMENT OF COMMERCE
Patent and Trademark OfficeAttorney's Docket Number
101-9409JSerial No.
10/**INFORMATION DISCLOSURE STATEMENT
BY APPLICANT**

(Use several sheets if necessary)

Applicant(s): **Kawasaki et al.**Filing Date: **April 13, 2004**Group Art Unit: **2154****U.S. PATENT DOCUMENTS**

*EXAMINER INITIAL	DOCUMENT NUMBER							DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	4	4	9	1	9	0	7		Koeppen et al.			
	4	6	2	6	9	8	5	12/86	Briggs	395	800-4	
	4	6	4	9	5	1	1	3/87	Gdula	711	106	
	4	6	7	0	8	3	8	6/87	Kawata	714	38	
	4	7	9	4	5	2	4	12/88	Carberry et al.	712	32	
	4	8	7	0	5	6	2	9/89	Kimoto et al.	711	167	
	4	9	1	8	6	5	0	4/90	Wolf	710	129	
	4	9	3	5	8	6	7	6/90	Wang et al.	711	217	
	4	9	7	5	5	9	3	12/90	Kurakazu et al.	327	141	
	4	9	8	4	1	9	5	1/8/91	Nakamura et al.	364	200	6/2/88
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	5	1	5	5	8	1	9	10/92	Watkins et al.	395	800-36	
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	DOCUMENT NUMBER							DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
	0	2	1	2	6	4	0	04/87	EUROPE- Kelda et al.			YES NO
	0	3	4	6	9	1	7	12/89	EUROPE	G06F	13/28	X
	0	5	0	6	5	9	4	9/92	EUROPE	G06F	3/12	X
	0	5	2	3	7	6	4	1/93	EUROPE	G06F	13/28	X
	0	5	8	8	6	0	7	3/94	EUROPE	G06F	15/78	X
	0	6	2	4	8	4	4	11/94	EUROPE	G06F	12/08	X
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)												
		IEEE Journal of Solid-State Circuits, Vol. 26, No. 11, November 11, 1991, pp. 1586-92, "A 0.5W 64-Kilobyte Snoopy Cache Memory with										
		Pseudo Two-Port Operation" by Kobayashi et al.										
		Proceedings, IEEE 1993 Custom Integrated Circuits Conference, May 9, 1993, pp. 25.21-25.24, "A High Performance/Low Power K-byte 4-Way										
		Set Associative Integrated Cache Memory," by Nguyen et al.										
		IBM Technical Disclosure Bulletin, November 1989, Vol. 32, No. 6A, pp. 246-248, "Method of Communication Between a PC and a 68000-										
		Based System Using Parallel Ports."										
EXAMINER									DATE CONSIDERED			
*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.												